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(71) Applicant

General Electric Company

(Incorporated in the USA - New York)

One River Road, Schenectady,
12345 New York, United States of America

(72) Inventors

Ching Yeu Wei
George Edward Possin
Robert Forrest Kwasnick

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(74) Agent and/or Address for Service

R W Pratt
General Electric Technical Services Company Inc,
London Patent Operation, Essex House,
12/13 Essex Street, London WC2R 3AA,
United Kingdom

(54) Positive control of the source/drain-gate overlap in self-aligned TFTs via a top hat gate electrode configuration

(57) Positive control over the length of the overlap between the gate electrode (18) and the source and drain electrodes (36) in a thin film transistor is provided by a gate conductor layer (18) comprising two different conductors (14,16) having differing etching characteristics. As part of the gate conductor pattern definition process, both gate conductors (14,16) are etched back to expose the first gate conductor layer (14) in accordance with the desired overlap between the gate electrode (18) and the source and drain electrodes (36). Thereafter, the remainder of the device is fabricated with the source and drain electrodes (36) self-aligned with respect to the second gate conductor layer (14) using a planarization and non-selective etch method.

